WHAT IS CLAIMED IS:

1. A logic apparatus comprising:

a semiconductor substrate;

a first single-electron device comprising a first conductive island insulatively disposed over the semiconductor substrate, at least two first tunnel barriers insulatively disposed over the semiconductor substrate, the first conductive island being interposed between the first tunnel barriers, first and second electrodes insulatively disposed over the semiconductor substrate, the first conductive island being coupled with the first and second electrodes through the first tunnel barriers, respectively, and a first charge storage region insulatively disposed over the first conductive island; and

a second single-electron device comprising a second conductive island insulatively disposed over the semiconductor substrate, at least two second tunnel barriers insulatively disposed over the semiconductor substrate, the second conductive island being interposed between the second tunnel barriers, third and fourth electrodes insulatively disposed over the semiconductor substrate, the second conductive island being coupled with the third and fourth electrodes through the second tunnel barriers, respectively, and a second charge storage region insulatively disposed over the second conductive island, the third electrode of

the second-single electron device being connected to the first electrode of the first single-electron device.

2. A logic apparatus according to claim 1, which includes an output amplifier connected to the first electrode of the first single-electron device and the third electrode of the single-electron device.

3. A logic apparatus according to claim 1, wherein the first and second single-electron devices include fifth and sixth electrodes insulatively disposed over the first and second charge storage regions, and logic signals are input to the fifth and sixth electrodes of the first and second single-electron devices, a logic operation result is output from the first and third electrodes.

4. A logic apparatus according to claim 3, wherein the first electrode and the third electrode are formed of a common electrode region.

5. A logic apparatus according to claim 1, wherein the first and second single-electron devices include fifth and sixth electrodes insulatively disposed over the first and second charge storage regions, logic signals are input to the fifth and the sixth electrode of the first and the second single-electron device, a logic operation result is output from the second electrode of the first single-electron device.

6. A logic apparatus according to claim 5, wherein the first electrode and the third electrode are formed of a common electrode region.

7. A logic apparatus according to claim 1, wherein each of the first and second single-electron devices has a logical inversion relation between a state that charges are accumulated in the charge storage region and a state that no charge is accumulated therein.

8. A logic apparatus according to claim 1, which includes an element configured to inject charges to the charge storage region or extract charges therefrom.

9. A logic apparatus according to claim 1, which an element configured to generate a potential difference between the conductive island and the charge storage regions, to inject charges to the charge storage region or extract charges therefrom.

10. A logic apparatus according to claim 1, wherein a Coulomb oscillation in a state that charges are accumulated in the charge storage region is shifted by a half period from that in a state that no charge is accumulated therein.

11. A logic apparatus according to claim 10, wherein a size and materials of the conductive island are selectively set to shift the Coulomb oscillation by a half period between a state that charges are accumulated in the charge storage region and a state

that no charge is accumulated therein.

12. A logic apparatus according to claim 1, which includes a resistor between a node of the first electrode of the first single-electron device and the third electrode of the second single-electron device and a voltage source and wherein the second electrode of the first single-electron device and the fourth electrode of the second single-electron device are grounded.

13. A logic apparatus comprising a plurality of single-electron device pairs each including the first and second single-electron devices according to claim 1, the first and second single-electron device pairs being connected in parallel or serial.

14. A logic apparatus comprising a plurality of single-electron device pairs each including the first and second single-electron devices according to claim 1, the first and second single-electron device pairs being connected in parallel and serial.

15. A logic circuit comprising:

a first logic circuit using a single-electron device occurring an oscillation according to a voltage and having a capacitor configured to selectively store charges, a first terminal, a second terminal and a third terminal;

a second logic circuit using a single-electron device occurring an oscillation according to a voltage

and having a capacitor configured to selectively store charges, a first terminal connected to the first terminal of the first logic circuit, a second terminal and a third terminal;

a resistor connected to a node of the first terminals of the first and second logic circuits and a voltage source;

a ground terminal connected to the second terminals of the first and second logic circuits; and

logical signal input terminals connected to the third terminals of the first and second logic circuits to be inputted with logical signals.

16. A logic circuit according to claim 15, which includes an output amplifier connected to the node of the first terminals of the first and second logic circuit.

17. A logic circuit according to claim 15, wherein a logic operation result is output from the first terminals of the first and second logic circuits.

18. A logic circuit according to claim 15, wherein a logic operation result is output from the second terminal of the first logic circuit.

19. A logic circuit according to claim 15, wherein each of the first and second logic circuits has a logical inversion relation between a state that charges are accumulated in the capacitor and a state that no charge is accumulated therein.

20. A logic circuit according to claim 15, which includes a circuit configured to inject charges to the capacitor or extract charges therefrom.

21. A logic circuit comprising a plurality of logic circuit pairs each including the first and second logic circuits according to claim 15, the first and second logic circuits being connected in parallel or serial.

22. A logic circuit comprising a plurality of logic circuit pairs each including the first and second logic circuits according to claim 15, the first and second logic circuits being connected in parallel and serial.